- **High-Speed Output Circuit to Drive PNP Power Transistor**
- **Precision Reference Voltage . . . 1.5 V ±2% at T_A = 25°C**
- **Oscillator Frequency . . . 50 kHz to 0.8 MHz**
- **Low Supply Voltage Operation V_{CC} = 2.5 V to 12 V**
- **Output Voltage Limit (Channel 5 and 6)**
- **Low Supply Current**
- **Internal Undervoltage Lockout Protection**
- **Internal Short-Circuit Protection**
- **Shutdown Function**
- **External Sink Current Setting on Output Stage**

description

The TL1466I is a six channel pulse-width-modulation (PWM) control circuit. This device contains reference voltage with a precision of ±2%, a triangle wave oscillator capable of high frequency oscillation up to 0.8 MHz, various protection circuitry, and shutdown circuitry. The output regulation voltage for each channel is set by an external resistor divider. Moreover, the output stage is capable of driving a PNP power transistor with high speed. The high frequency/efficiency switching operation eliminates switching loss by using internal over-drive circuitry at the rising edge and with reverse bias connecting external bootstrap capacitor at the falling edge. The MOSFET can be used in parallel with the output diode at channel 1 and 4. This results in further high efficiency operation replacing the constant time with this MOSFET when the output diode is turned on. Furthermore, it operates 2.5 V supply voltage and balances switching current by switching repeatedly at the reverse phase with two pairs (channel 1, 4, 6, and 2, 3, 5) of the six channels. The oscillator output of channel 1, 4, and 6 is reverse phase for channel 2, 3, and 5. As a result of these features, this device is well-suited for power supply of portable systems in battery-powered equipment.

FUNCTION TABLE FOR STANDBY

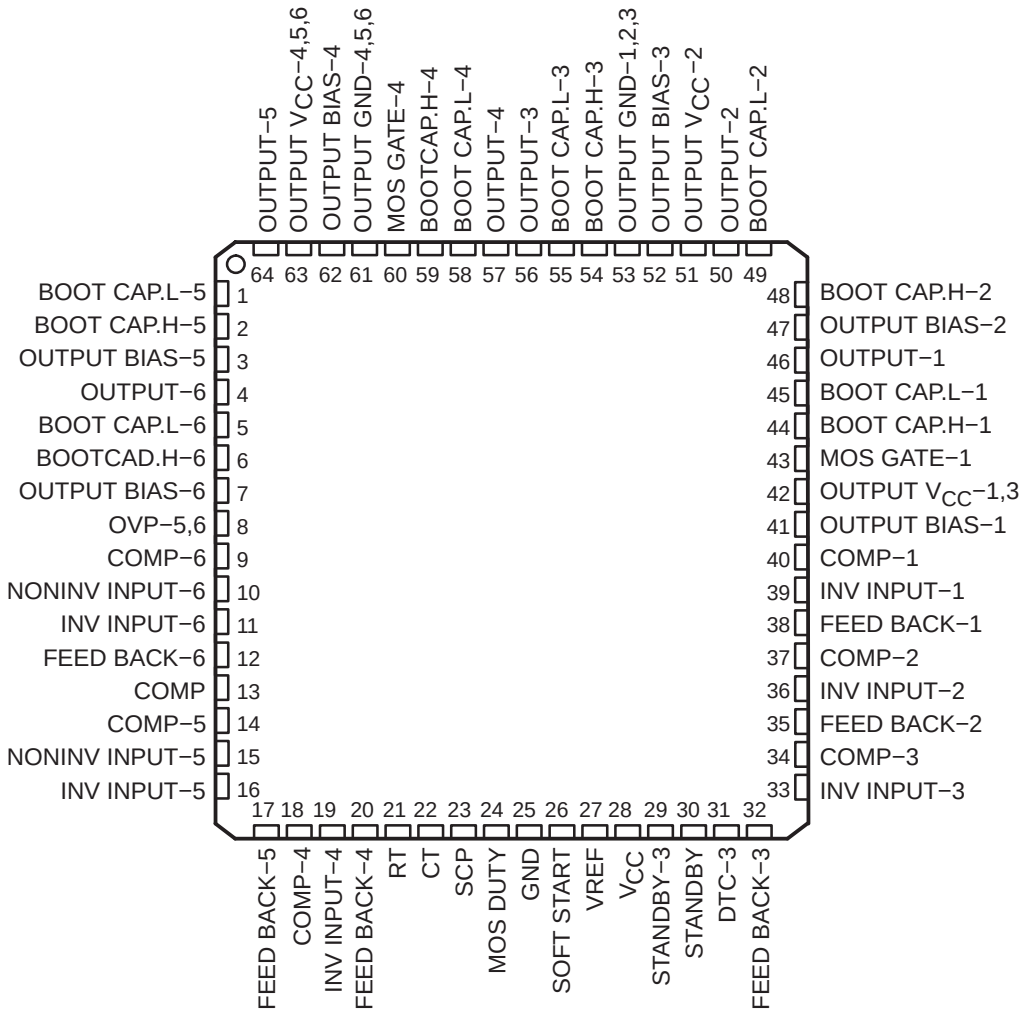
INPUT		OUTPUT		
STANDBY	**STANDBY-3**	**VREF**	**OUTPUT1, 2, 4, 5, 6**	**OUTPUT3**
$V_I \le 0.4$ V	X†	OFF	OFF	OFF
$V_I \ge 2$ V	$V_I \ge 2$ V	ON	ON	ON
	$V_I \le 0.4$ V	ON	ON	OFF

† X: High-level or low-level

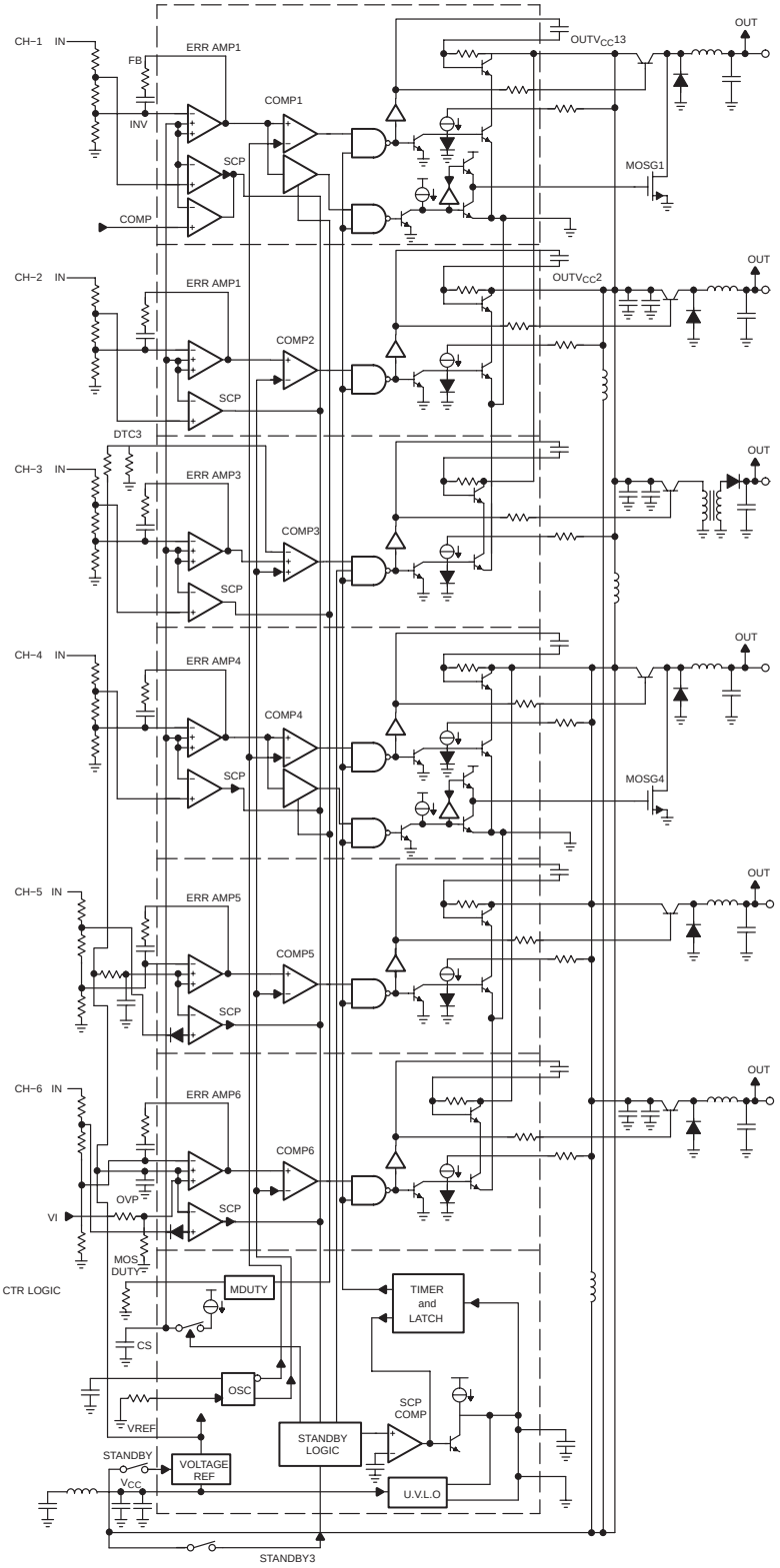
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

pin assignments

PM PACKAGE
(TOP VIEW)



functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
BOOT CAP.H−1	44	Bootstrap capacitor connection. The connection allows reverse-bias for external PNP transistor of channel 1.
BOOT CAP.L−1	45	
BOOT CAP.H−2	48	Bootstrap capacitor connection. The connection allows reverse-bias for external PNP transistor of channel 2.
BOOT CAP.L−2	49	
BOOT CAP.H−3	54	Bootstrap capacitor connection. The connection allows reverse-bias for external PNP transistor of channel 3
BOOT CAP.L−3	55	
BOOT CAP.L−4	58	Bootstrap capacitor connection. The connection allows reverse-bias for external PNP transistor of channel 4.
BOOT CAP.H−4	59	
BOOT CAP.L−5	1	Bootstrap capacitor connection. The connection allows reverse-bias for external PNP transistor of channel 5.
BOOT CAP.H−5	2	
BOOT CAP.L−6	5	Bootstrap capacitor connection. The connection allows reverse-bias for external PNP transistor of channel 6.
BOOT CAP.H−6	6	
COMP	13	Output regulation voltage monitor terminal. When this terminal voltage drops below VREF voltage (1.5 V), charging to capacitor connected to SCP terminal (pin 23) is initiated.
COMP−1	40	Output regulation voltage monitor terminal (channel 1). When this terminal voltage drops below VREF voltage (1.5 V) charging to capacitor connected to SCP terminal (pin 23) is initiated.
COMP−2	37	Output regulation voltage monitor terminal (channel 2). When this terminal voltage drops below VREF voltage (1.5 V) charging to capacitor connected to SCP terminal (pin 23) is initiated.
COMP−3	34	Output regulation voltage monitor terminal (channel 3). When this terminal voltage drops below VREF voltage (1.5 V), charging to capacitor connected to SCP terminal (pin 23) is initiated.
COMP−4	18	Output regulation voltage monitor terminal (channel 4). When this terminal voltage drops below VREF voltage (1.5 V) charging to capacitor connected to SCP terminal (pin 23) is initiated.
COMP−5	14	Output regulation voltage monitor terminal (channel 5). When this terminal voltage drops below NONINV INPUT−5 terminal voltage − 0.55 V, charging to capacitor connected to SCP terminal (pin 23) is initiated.
COMP−6	9	Output regulation voltage monitor terminal (channel 6). When this terminal voltage drops below NONINV INPUT−6 terminal voltage − 0.55 V, charging to capacitor connected to SCP terminal (pin 23) is initiated.
CT	22	Timing capacitor connection for oscillation frequency setting.
DTC−3	31	Dead-time control input for channel 3. The maximum ON duty cycle for OUTPUT−3 terminal is determined by comparing the input voltage of this terminal with the oscillator output (triangle wave).
FEEDBACK−1	38	Error amplifier output terminal (channel 1)
FEEDBACK−2	35	Error amplifier output terminal (channel 2)
FEEDBACK−3	32	Error amplifier output terminal (channel 3)
FEEDBACK−4	20	Error amplifier output terminal (channel 4)
FEEDBACK−5	17	Error amplifier output terminal (channel 5)
FEEDBACK−6	12	Error amplifier output terminal (channel 6)
GND	25	Logic ground
INV INPUT−1	39	Error amplifier inverting input terminal (channel 1)
INV INPUT−2	36	Error amplifier inverting input terminal (channel 2)
INV INPUT−3	33	Error amplifier inverting input terminal (channel 3)
INV INPUT−4	19	Error amplifier inverting input terminal (channel 4)
INV INPUT−5	16	Error amplifier inverting input terminal (channel 5)
INV INPUT−6	11	Error amplifier inverting input terminal (channel 6)
MOS DUTY	24	N-channel MOSFET ON duty cycle setting for the synchronous rectification of channel 1 and 4. The MOSFET ON duty cycle for the synchronous rectification is determined by the resistor value connected between this terminal and GND.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
MOS GATE−1	43	N-Channel MOSFET gate drive for the synchronous rectification of channel 1. The ON duty cycle for this terminal is determined by the resistor value connected to MOS DUTY (pin 24).
MOS GATE−4	60	N-Channel MOSFET gate drive for the synchronous rectification of channel 4. The ON duty cycle for this terminal is determined by the resistor value connected to MOS DUTY (pin 24).
NONINV INPUT−5	15	Error amplifier noninverting input terminal (channel 6). By connecting resistor and capacitor to this terminal, soft start function is accomplished increasing this terminal voltage slowly.
NONINV INPUT−6	10	Error amplifier noninverting input terminal (channel 6). By connecting resistor and capacitor to this terminal, soft start function is accomplished increasing this terminal voltage slowly.
OUTPUT−1	46	Output terminal to drive base for external PNP transistor of channel 1.
OUTPUT−2	50	Output terminal to drive base for external PNP transistor of channel 2.
OUTPUT−3	56	Output terminal to drive base for external PNP transistor of channel 3.
OUTPUT−4	57	Output terminal to drive base for external PNP transistor of channel 4.
OUTPUT−5	64	Output terminal to drive base for external PNP transistor of channel 5.
OUTPUT−6	4	Output terminal to drive base for external PNP transistor of channel 6.
OUTPUT BIAS−1	41	Resistor connection to set output sink current for OUTPUT−1 terminal (pin 46) of channel 1.
OUTPUT BIAS−2	47	Resistor connection to set output sink current for OUTPUT−2 terminal (pin 50) of channel 2.
OUTPUT BIAS−3	52	Resistor connection to set output sink current for OUTPUT−3 terminal (pin 56) of channel 3.
OUTPUT BIAS−4	62	Resistor connection to set output sink current for OUTPUT−4 terminal (pin 57) of channel 4.
OUTPUT BIAS−5	3	Resistor connection to set output sink current for OUTPUT−5 terminal (pin 64) of channel 5.
OUTPUT BIAS−6	7	Resistor connection to set output sink current for OUTPUT−6 terminal (pin 4) of channel 6.
OUTPUT GND−1,2,3	53	Ground for channel 1, 2, and 3 output.
OUTPUT GND−4,5,6	61	Ground for channel 4, 5, and 6 output.
OUTPUT V_{CC}−1,3	42	Supply voltage for channel 1 and 3 outputs.
OUTPUT V_{CC}−2	51	Supply voltage for channel 2 output.
OUTPUT V_{CC}−4,5,6	63	Supply voltage for channel 4, 5, and 6 outputs.
OVP−5,6	8	Over-voltage threshold voltage setting for output regulation voltage of channel 5 and 6.
RT	21	Timing resistor connection for oscillation frequency setting.
SCP	23	Capacitor connection for short-circuit protection. When voltage across COMP terminal for each channel is dropped below the specified threshold voltage, the capacitor connected between SCP and GND is charged by the constant current source (2.5 μA Typ). If the voltage reaches to 1.5 V, the timer latch circuitry is set and all channel outputs are forced to turn off.
SOFT START	26	Soft start operation for channel 1 to 4. By connecting a capacitor between this terminal connected internally to error amplifier noninverting input for channel 1 to 4 and GND, soft start operation is enabled charging a capacitor with the constant current source (3 μA Typ). Moreover, the same soft start operation is also enabled at the standby release using STANDBY−3 terminal only for channel 3.
STANDBY	30	ON/OFF common control input for all channels. The all channels output is turned off by adding low-level input voltage (0.4 V Max) to this terminal, and the reference voltage is also shutdown.
STANDBY−3	29	ON/OFF control input for channel 3. The channel 3 output is turned off by adding low-level input voltage (0.4 V Max) to this terminal.
V_{CC}	28	Supply voltage
VREF	27	1.5 V reference voltage output

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 13 V
Input voltage, V_I at OVP, COMP . . . . . 13 V
Error amplifier input voltage, $V_{(AMP)}$ . . . . . 13 V
Output voltage, V_O . . . . . 13 V
Peak output sink current, $I_{(SINK)}$ . . . . . 100 mA
Peak output source current, $I_{(SOURCE)}$ . . . . . −0.5 A
Continuous power total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1785 mW
Operating free-air temperature range, T_A . . . . . −20°C to 75°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to GND.
2. Device mounted on a 50 mm × 1.6 mm, fFR4 printed-circuit board.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		2.5		12	V
High-level standby input voltage (pin 29, 30), $V_{I(HS)}$		2		V_{CC}	V
Low-level standby input voltage (pin 29, 30), $V_{I(LS)}$				0.4	V
Output voltage, V_O				12	V
Current into feedback terminal, I_{OAMP}	Channel 1, 4			−30	µA
	Channel 2, 3, 5, 6			−45	
Feedback capacitance, $C_{(NF)}$		0.5	5	100	nF
Bootstrap capacitance, $C_{(BOOT)}$		100	500		pF
Bias resistor, $R_{(BIAS)}$		3		20	kΩ
Timing resistor, $R_{(T)}$		12		100	kΩ
Timing capacitor, $C_{(T)}$		68		1000	pF
Oscillator frequency, $f_{(osc)}$		0.05		0.8	MHz
Operating free-air temperature, T_A		−20		75	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 0.43 MHz (unless otherwise noted)

reference section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref}	Output voltage (pin 27)	T_A = 25°C, I_{OR} = −1 mA	1.47	1.50	1.53	V
$R_{(EGIN)}$	Line regulation	V_{CC} = 2.5 V to 12 V, I_{OR} = −1 mA		2	12.5	mV
$R_{(EGL)}$	Load regulation	I_{OL} = −0.1 mA to −1 mA		1	7.5	mV
$V_{(RTC1)}$	Output voltage change with temperature	T_A = −20°C to 25°C		−0.2%	±2%	
$V_{(RTC2)}$		T_A = 25°C to 75°C		−0.2%	±2%	
I_{OS}	Short-circuit output current	V_{ref} = 0 V	−4	−20		mA

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 0.43 MHz (unless otherwise noted) (continued)

undervoltage lockout section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(th)}$	High-level threshold voltage	T_A = 25°C		2.45		V
$V_{(tl)}$	Low-level threshold voltage			2.35		V
V_{hys}	Hysteresis		0.05	0.1		V
$V_{(R)}$	Reset threshold voltage (V_{CC})		2.1	2.2		V

oscillator section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Oscillator frequency	$C_{(T)}$ = 100 pF, $R_{(T)}$ = 47 kΩ		0.43		MHz
$f_{(dev)}$	Standard deviation of frequency	All the values are constant		7%		
$f_{(dv)}$	Frequency change with voltage	V_{CC} = 2.5 V to 12 V		1%		
$f_{(dT1)}$	Frequency change with temperature	T_A = −20°C to 25°C		−0.5%	±4%	
$f_{(dT2)}$		T_A = 20°C to 75°C		0.5%	±4%	

output voltage monitor section

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(tOM)}$	Input threshold voltage (COMP terminals: pin 13, 18, 34, 37, 40)		T_A = 25°C (channel 1, 2, 3, 4)	1.45	1.50	1.55	V
$V_{(IOOM)}$	Input offset voltage (pin 9, 14)		$V_{I(10, 15\ pin)}$ = 1.5 V, T_A = 25°C (channel 5,6)		0.55		V
$I_{(ICOMP)}$	Input bias current	Pin 13, 18, 34, 37, 40	V_I = 1 V		−0.8	−2	µA
		Pin 9, 14	V_I = 0.5 V, $V_{I(10, 15\ pin)}$ = 1.5 V				

short-circuit protection control section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(tPC)}$	Input threshold voltage (pin 23)	T_A = 25°C	1.45	1.53	1.61	V
$V_{(STBY)}$	UVLO standby voltage (pin 23)		20	60	100	mV
V_I	Latched input voltage (pin 23)			10	30	mV
$I_{(bPC)}$	Input source current (pin 23)	T_A = 25°C	−1	−2.5	−3.5	µA

dead-time control section (channel 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(Idt)}$	Input current (DTC−3 terminal: pin 31)	$V_{I(31\ pin)}$ = 0.5 V		−1	−6	µA
$V_{(t)}$	Input threshold voltage	Duty cycle = 0%	0.55	0.65	0.75	V
$V_{(t100)}$		Duty cycle = 100%	1.25	1.35	1.45	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f = 0.43 MHz (unless otherwise noted) (continued)

error-amplifier section

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(t)}$	Input threshold voltage	V_O = 1 V (channel 1, 2, 3, 4)		1.46	1.50	1.54	V
V_{IO}	Input offset current	V_O = 1 V (channel 5, 6)			5	40	mV
I_{IB}	Input bias current	V_O = 1 V	INV INPUT (pin 11, 16, 19, 33, 36, 39)		−200	−500	nA
			INV INPUT (pin 10, 15)		−0.9	−2.5	µA
V_{ICR}	Common-mode input voltage range	V_{CC} = 2.5 V to 12 V		0 to V_{CC}−1			V
$A_{(v)}$	Open-loop voltage amplification				70		dB
B1	Unity-gain bandwidth				6		MHz
V_{OM+}	Positive output voltage swing			V_{ref}−0.1			V
$V_{OM−}$	Negative output voltage swing					0.2	V
I_{OM+}	Output sink current	V_O = 1 V		0.5	2		mA
$I_{OM−}$	Output source current	V_O = 1 V	Channel 1, 4	−30	−80		µA
			Channel 2, 3, 5, 6	−45	−100		

output voltage limit section (channel 5, 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(tOV)}$	Input threshold voltage	$V_{I(10, 15 pin)}$ = 1 V	0.95	1	1.05	V
$V_{(BOV)}$	Input bias current	$V_{I(8 pin)}$ = 1.5 V, $V_{I(10, 15 pin)}$ = 1 V		−0.7	−2	µA

soft start section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(bss)}$	Input source current (pin 26)	STANDBY−3 terminal = 2 V SOFT START terminal = 1 V	−1	−2.5	−4	µA

MOSFET DUTY setting section (channel 1, 4)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$D_{(MOS)}$	ON DUTY	$V_{(FB)}$ = 1 V	R_{DUTY} = 5 kΩ		20%		
			R_{DUTY} = 25 kΩ		40%		

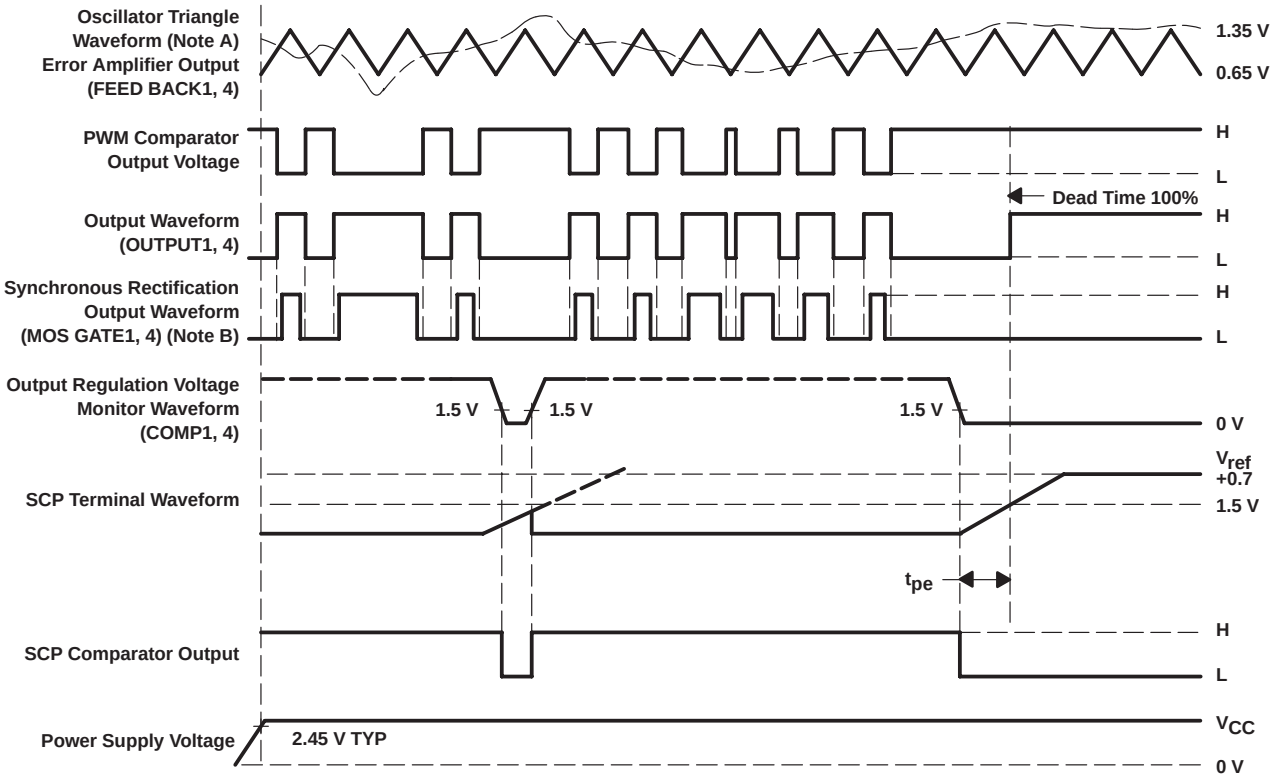
output section

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SINK)}$	Output sink current	$R_{(BIAS)}$ = 6.8 kΩ	6.3	8.5	10.7	mA
		$R_{(BIAS)}$ = 10 kΩ	4.5	6	7.5	
$I_{(GSOURCE)}$	MOS gate source current	$V_{O(43, 60 pin)}$ = 1 V, T_A = 25°C		−50		mA
$I_{(GSINK)}$	MOS gate sink current	$V_{O(43, 60 pin)}$ = 2 V, T_A = 25°C		50		mA
$I_{(GOH)}$	MOS gate high-level output voltage		3.5	4		V
$I_{(GOL)}$	MOS gate low-level output voltage			0.1	0.3	

total device

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(ccs)}$	Standby supply current	STANDBY terminal = 0 V		1	10	µA
$I_{(cca)}$	Average supply current	$R_{(T)}$ = 47 kΩ		6	9	mA

PARAMETER MEASUREMENT INFORMATION



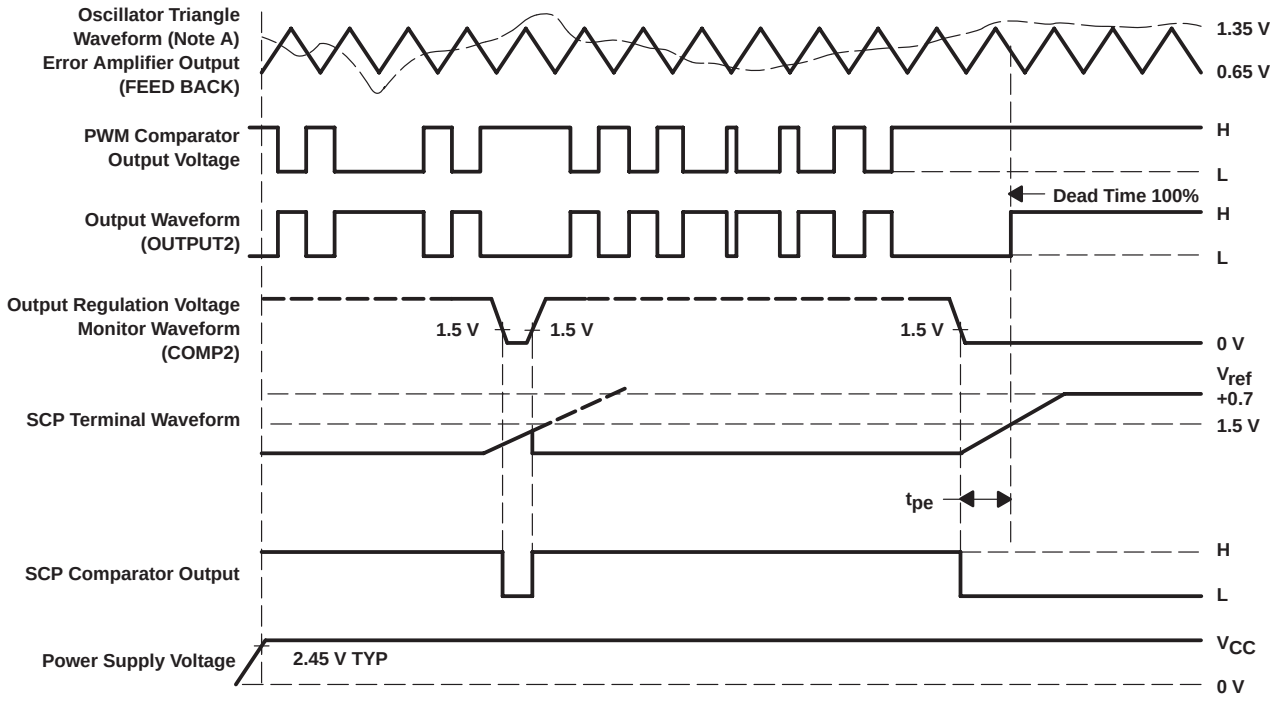
† Protection enable time, $t_{pe} = (588 \times 10^3 \times C_{pe})$ in seconds

NOTES: A. The oscillator output of channel 1, 4, and 6 is reverse phase for channel 2, 3, and 5.

B. The ON (high-level output state) time for the synchronous rectification output (MOS GATE1, 4) is determined by the resistor value connected to MOS DUTY terminal (pin 24) and this time is controlled internally without exceeding OFF (high-level output state) of output (OUTPUT1,4).

Figure 1. Timing Diagram (channel 1, 4)

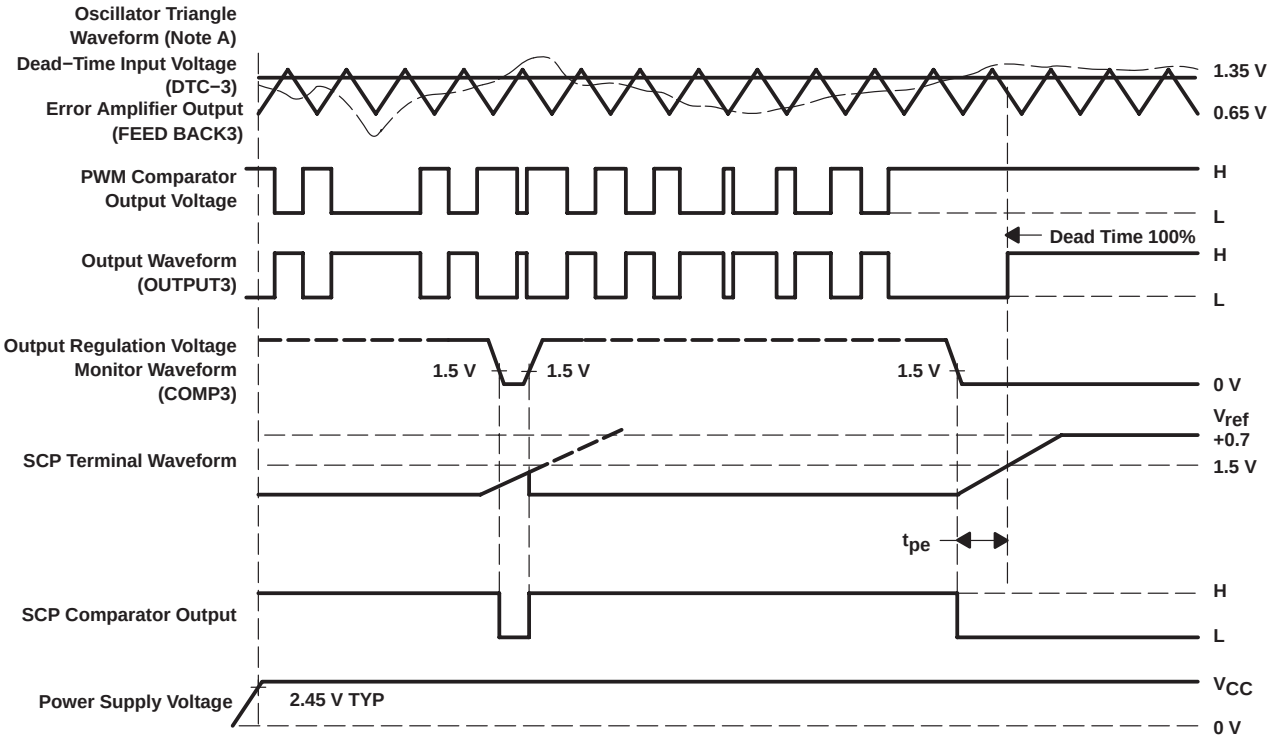
PARAMETER MEASUREMENT INFORMATION



† Protection enable time, $t_{pe} = (588 \times 10^3 \times C_{pe})$ in seconds
NOTE A: The oscillator output of channel 1, 4, and 6 is reverse phase for channel 2, 3, and 5.

Figure 2. Timing Diagram (channel 2)

PARAMETER MEASUREMENT INFORMATION

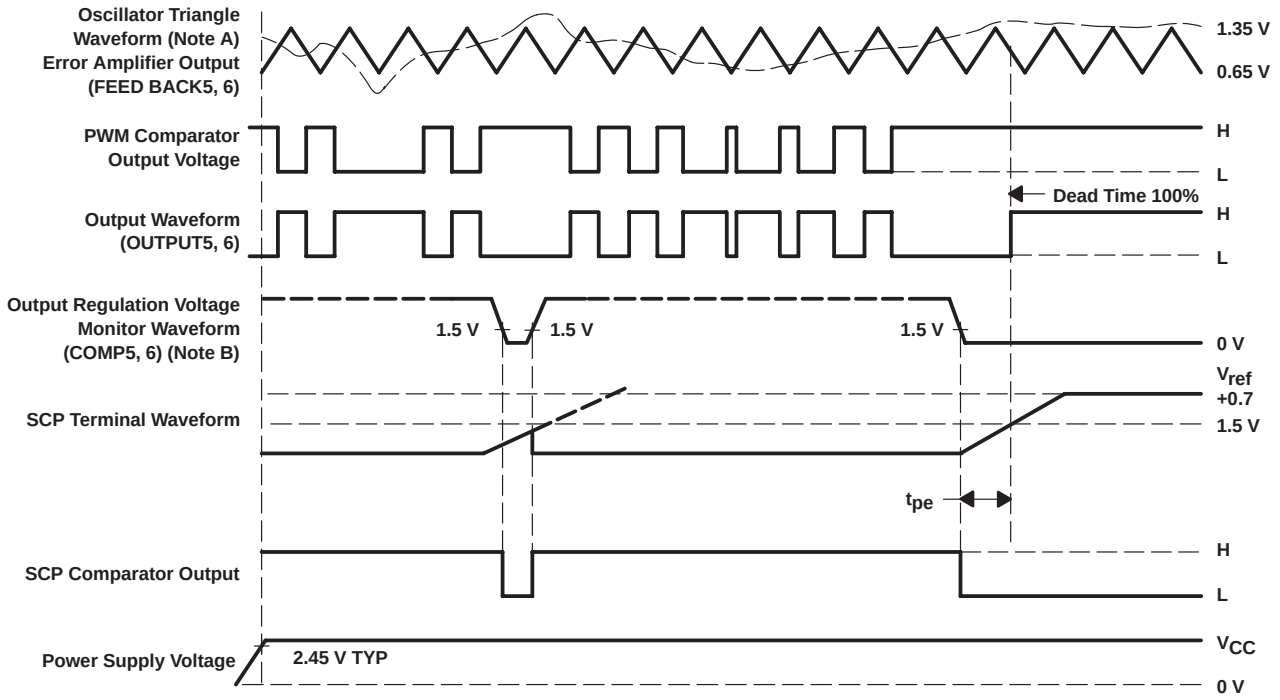


† Protection enable time, $t_{pe} = (588 \times 10^3 \times C_{pe})$ in seconds

NOTE A: The oscillator output of channel 1, 4, and 6 is reverse phase for channel 2, 3, and 5.

Figure 3. Timing Diagram (channel 3)

PARAMETER MEASUREMENT INFORMATION



† Protection enable time, $t_{pe} = (588 \times 10^3 \times C_{pe})$ in seconds

NOTES: A. The oscillator output of channel 1, 4, and 6 is reverse phase for channel 2, 3, and 5.

B. The threshold voltage at $V_{(A)}$ is set by following the formula below:
$V_{(A)}$ Input voltage of NONINV INPUT terminal (pin 10, 15) −0.55 V

Figure 4. Timing Diagram (channel 5, 6)

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

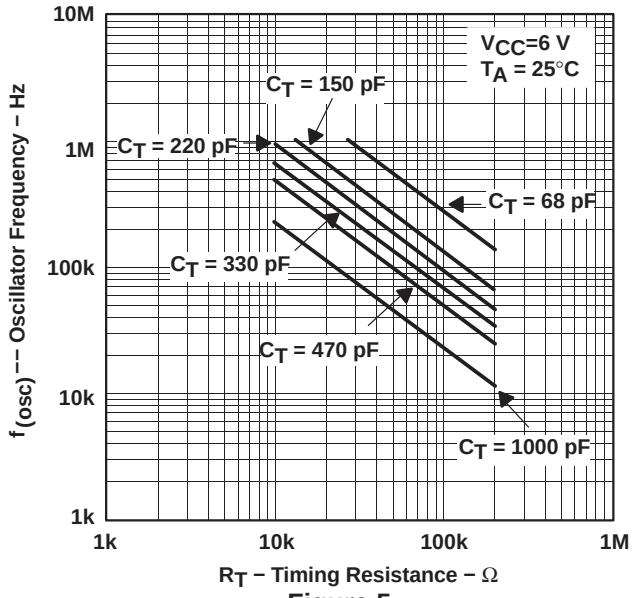


Figure 5

OSCILLATOR FREQUENCY vs FREE-AIR TEMPERATURE

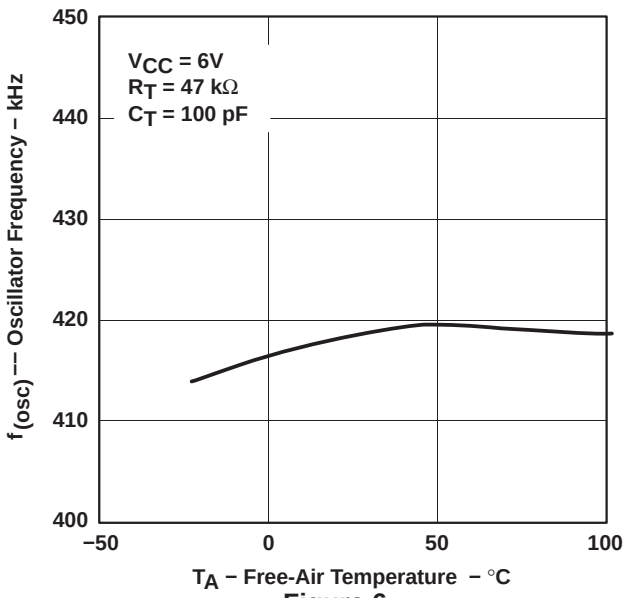


Figure 6

AVERAGE SUPPLY CURRENT vs FREE-AIR TEMPERATURE

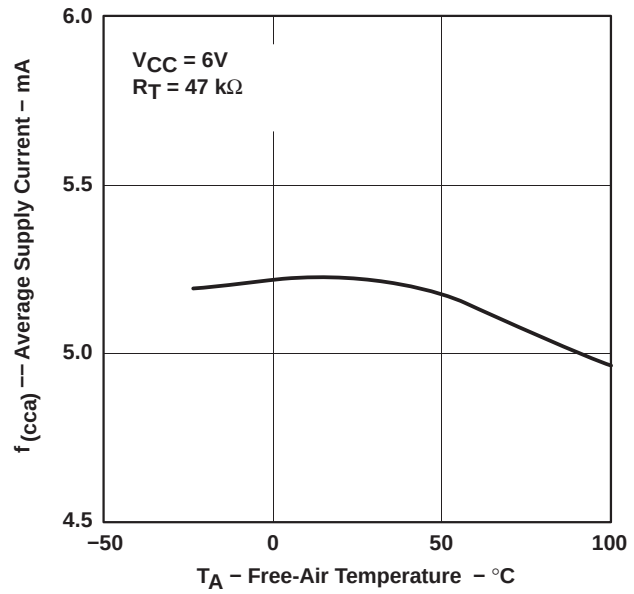


Figure 7

AVERAGE SUPPLY CURRENT vs SUPPLY VOLTAGE

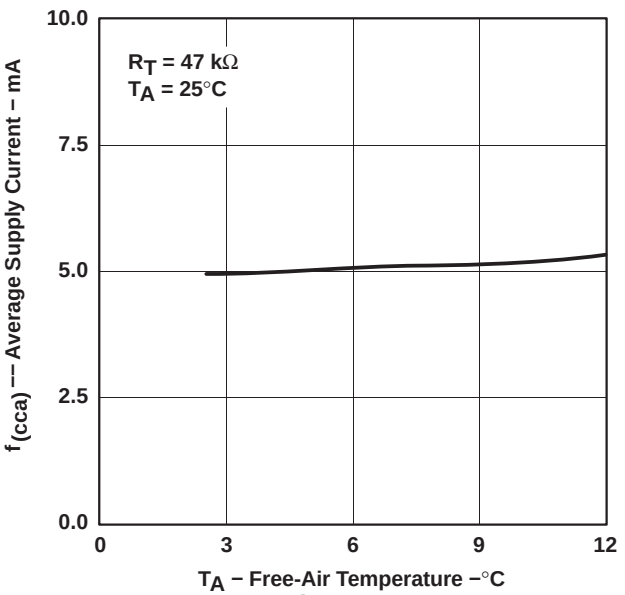


Figure 8

TYPICAL CHARACTERISTICS

VOLTAGE REFERENCE vs FREE-AIR TEMPERATURE

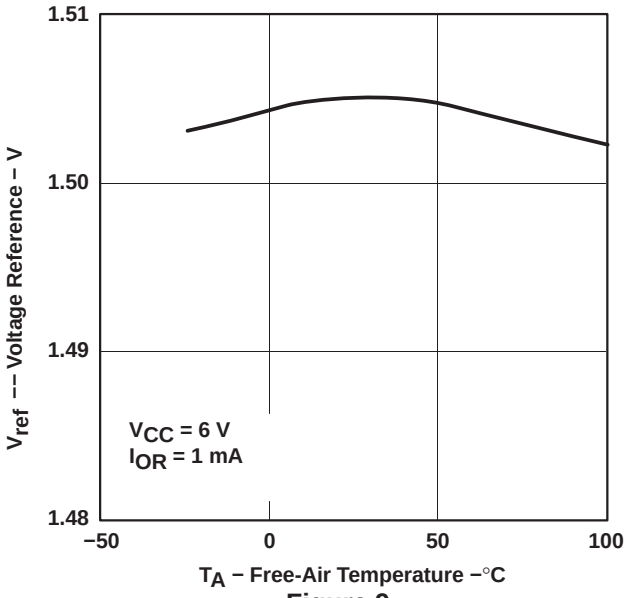


Figure 9

VOLTAGE REFERENCE vs SUPPLY VOLTAGE − 1

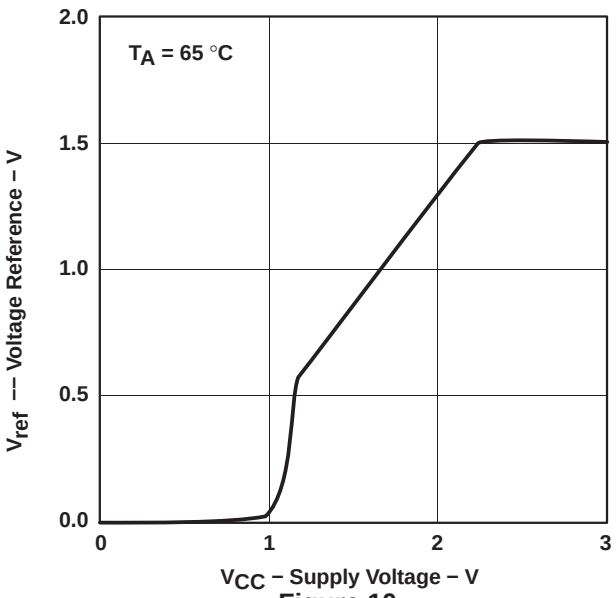


Figure 10

VOLTAGE REFERENCE vs SUPPLY VOLTAGE − 2

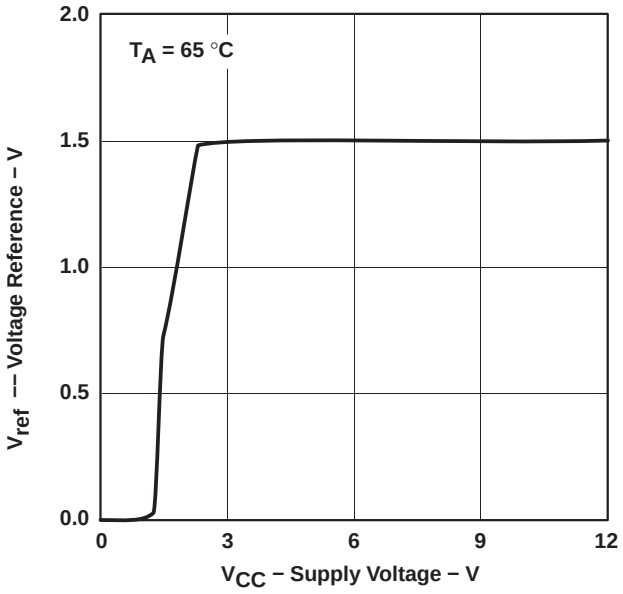


Figure 11

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT vs BIAS RESISTANCE

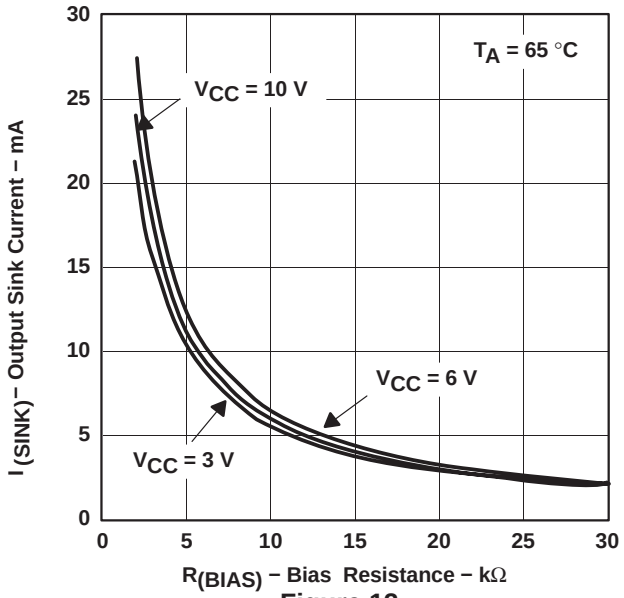


Figure 12

OUTPUT SINK CURRENT vs FREE-AIR TEMPERATURE

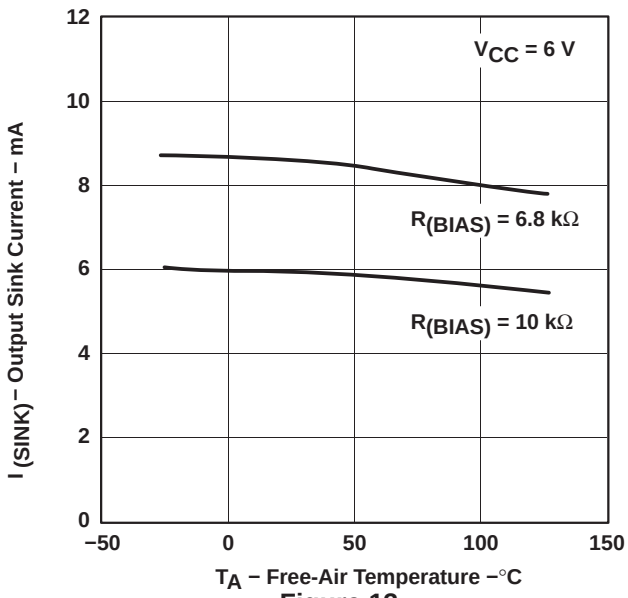


Figure 13

OUTPUT ON DUTY CYCLE vs DEAD-TIME INPUT VOLTAGE

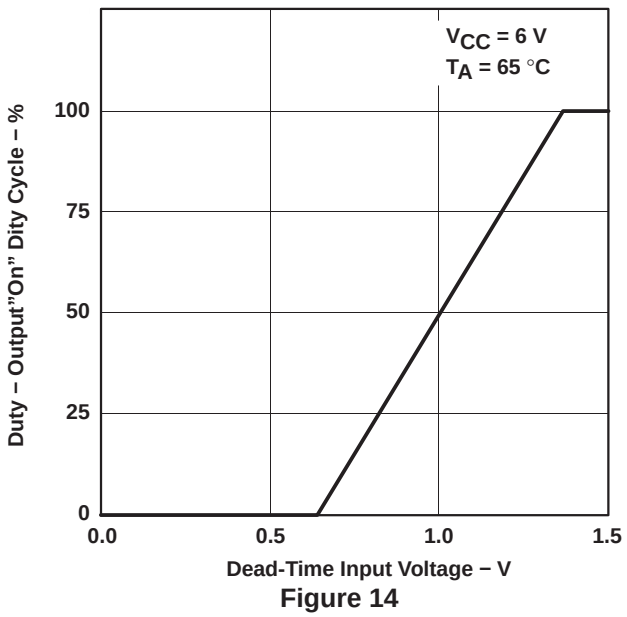


Figure 14

MOSFET ON DUTY CYCLE vs RESISTANCE

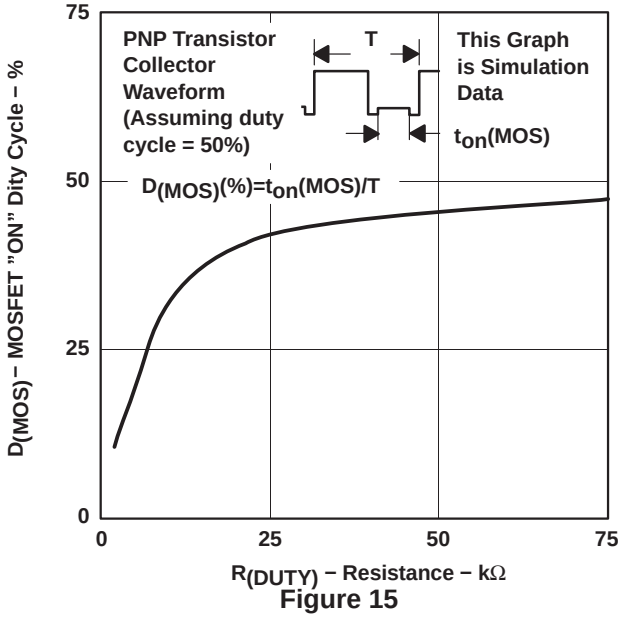


Figure 15

TYPICAL CHARACTERISTICS

MOSFET ON DUTY CYCLE vs FREE-AIR TEMPERATURE

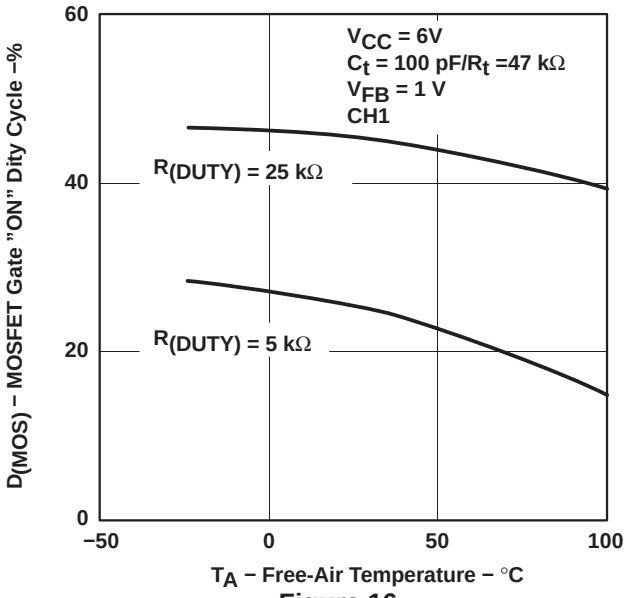


Figure 16

MOSFET GATE HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

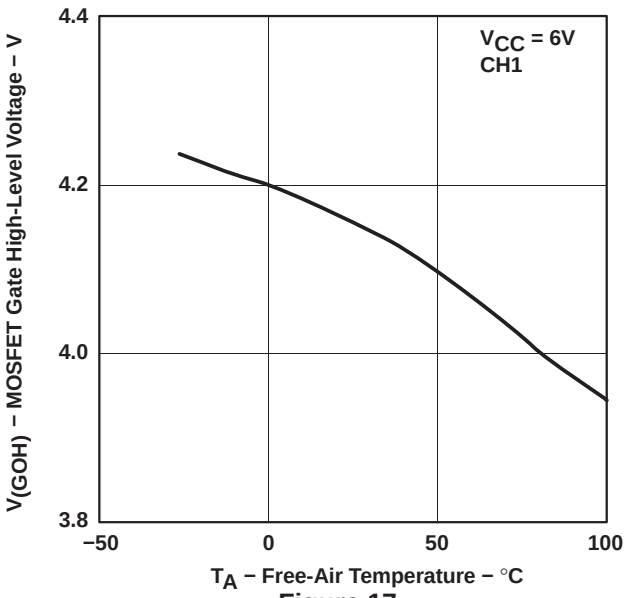


Figure 17

MOSFET GATE HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

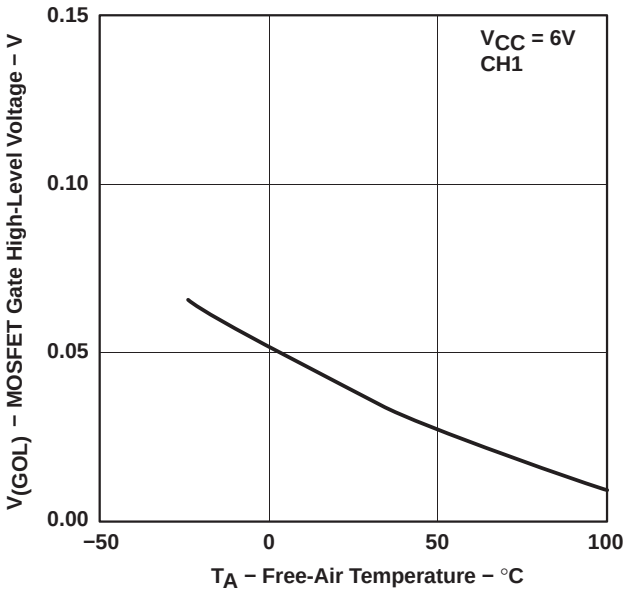


Figure 18

MOSFET GATE OUTPUT SOURCE CURRENT vs FREE-AIR TEMPERATURE

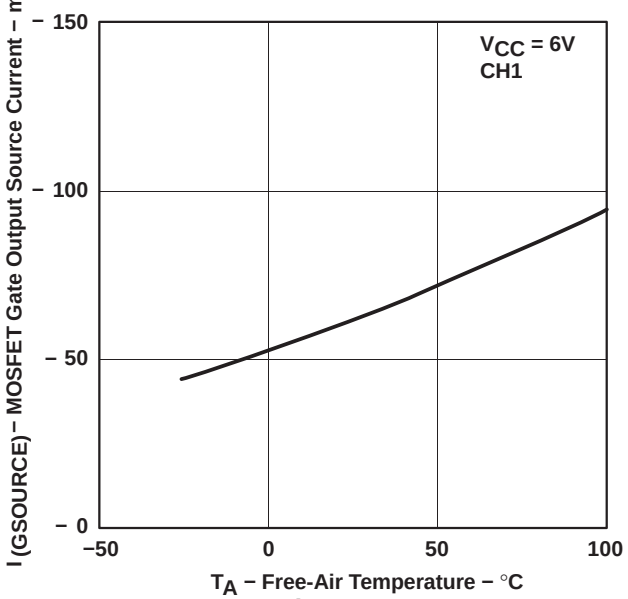


Figure 19

TYPICAL CHARACTERISTICS

MOSFET GATE OUTPUT SINK CURRENT vs FREE-AIR TEMPERATURE

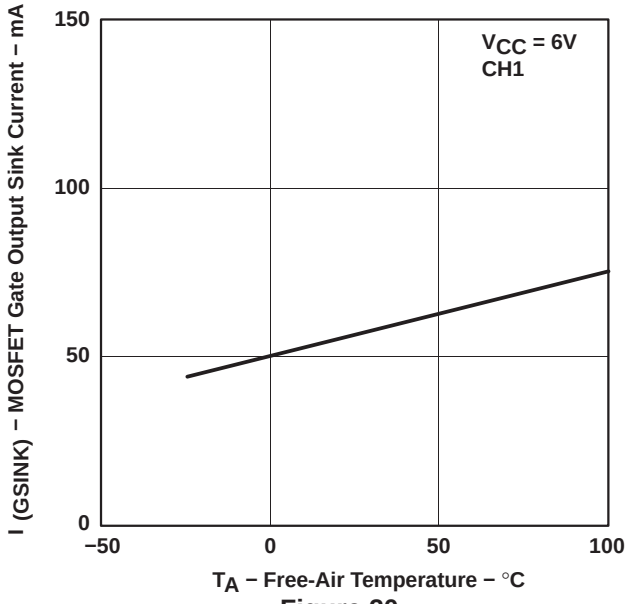


Figure 20

U.V.L.O THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

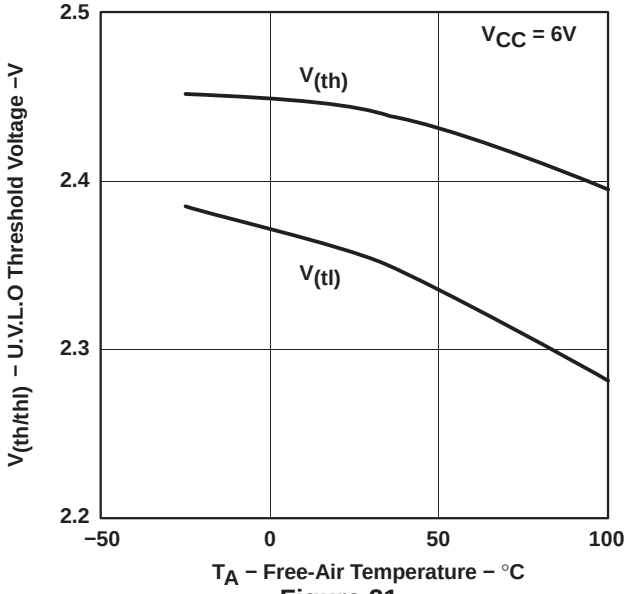


Figure 21

PWM COMPARATOR THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

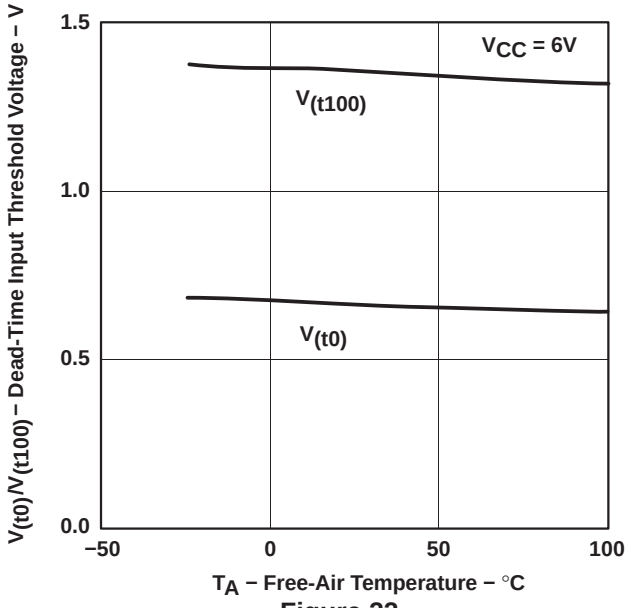


Figure 22

ERROR AMPLIFIER INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

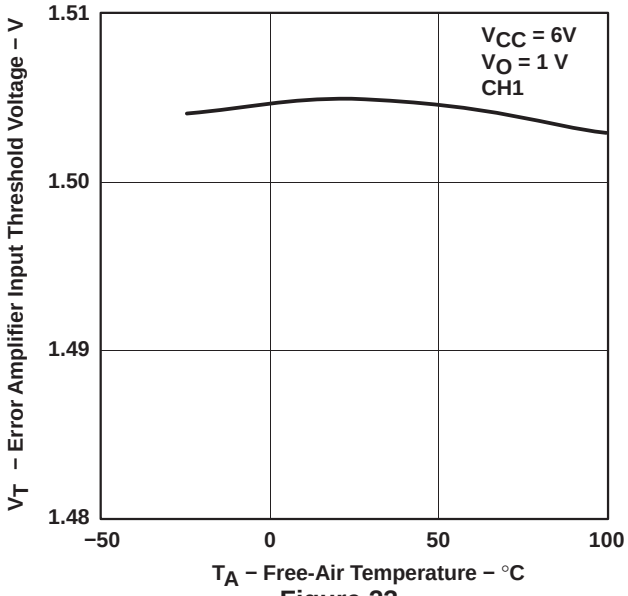


Figure 23

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

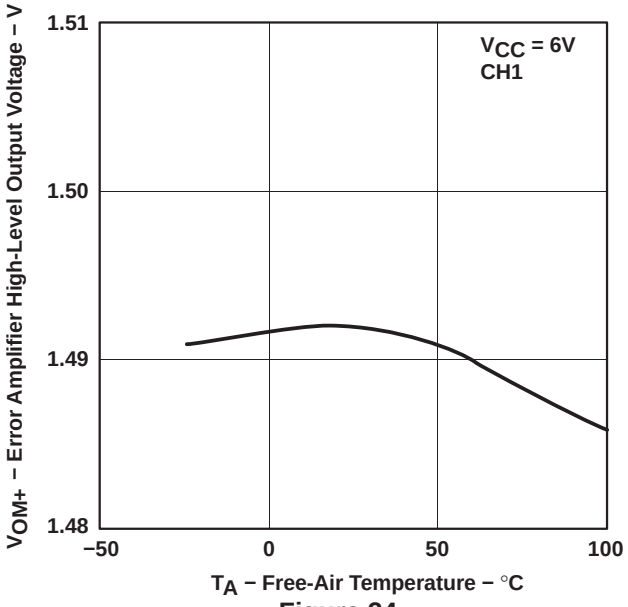


Figure 24

ERROR AMPLIFIER OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

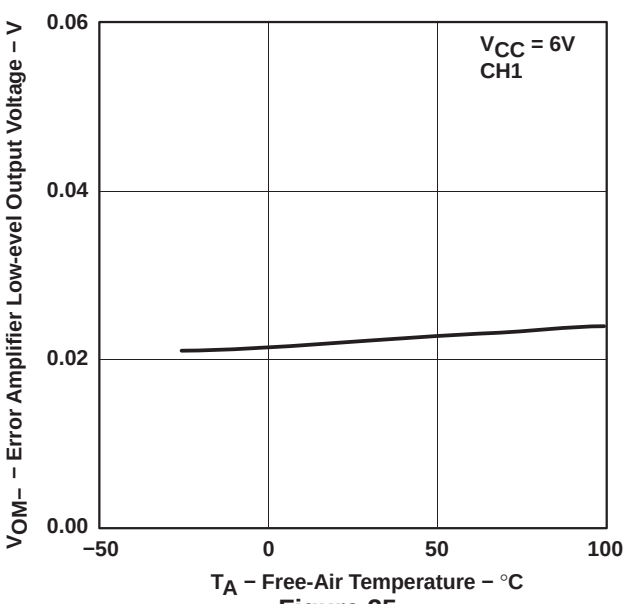


Figure 25

ERROR AMPLIFIER OUTPUT VOLTAGE vs OUTPUT SOURCE CURRENT

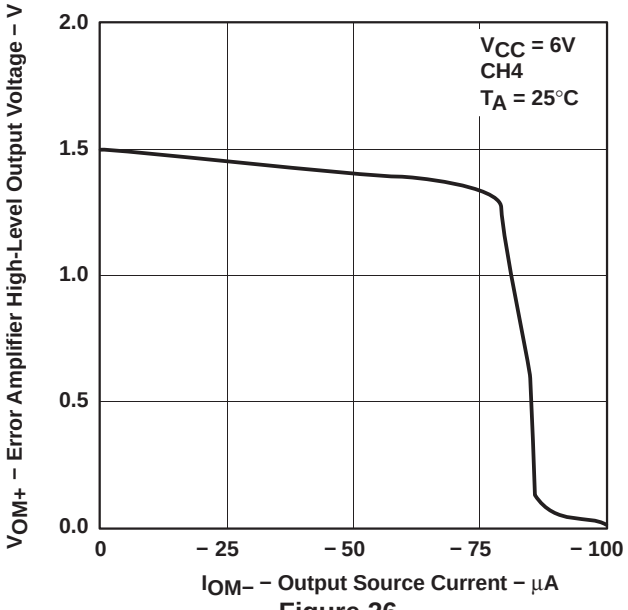


Figure 26

ERROR AMPLIFIER OUTPUT VOLTAGE vs OUTPUT SINK CURRENT

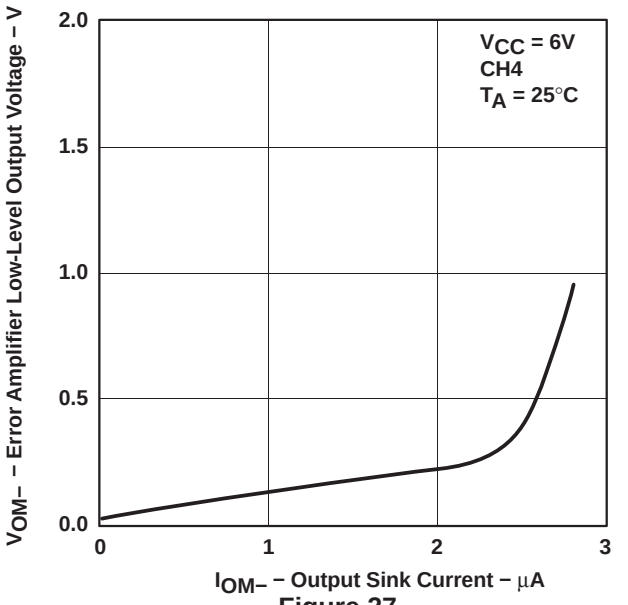


Figure 27

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OPEN-LOOP GAIN AND PHASE SHIFT vs FREE-AIR TEMPERATURE

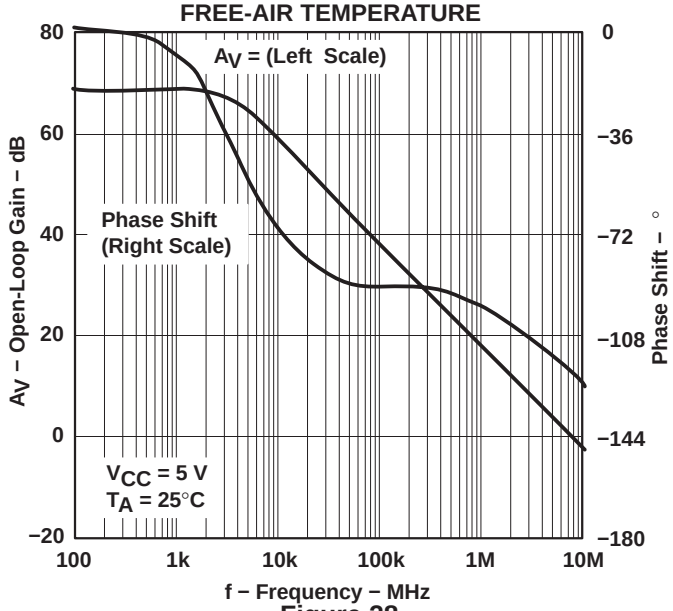


Figure 28

S.C.P INPUT SOURCE CURRENT vs FREE-AIR TEMPERATURE

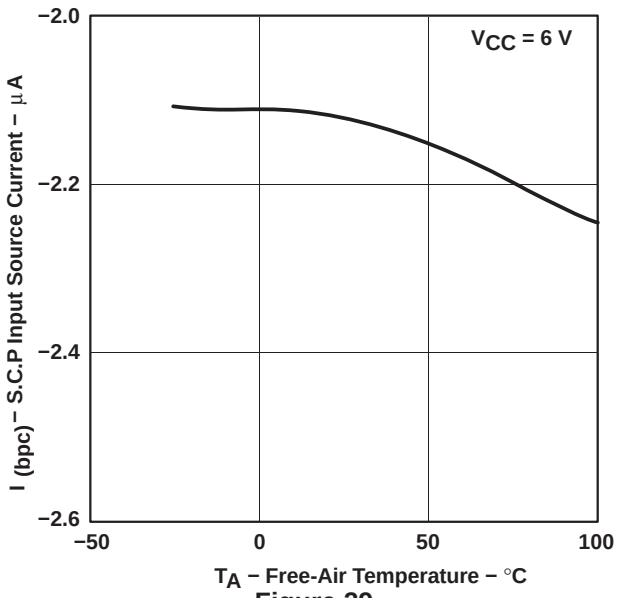


Figure 29

PROTECTION ENABLE TIME vs S.C.P CAPACITANCE

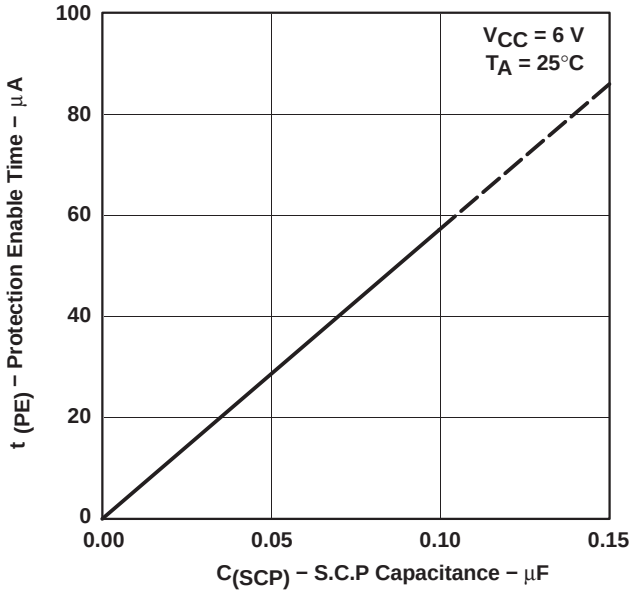


Figure 30

SOFT START TIME vs SOFT START CAPACITANCE

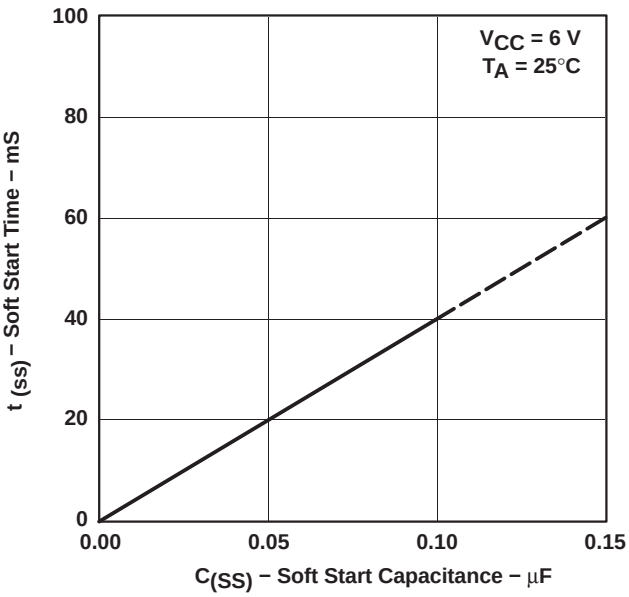


Figure 31

APPLICATION INFORMATION

bias resistance connection for output sink current setting

The bias resistance connection to set output sink current for each output of channel 1 through 6 (OUTPUT−1 to 6) should be connected as follows (refer to Figure 32):

- For channel 1 and 3, connect OUTPUT BIAS to OUTPUT V_{CC}−1,3 across bias resistance.
- For channel 2, connect OUTPUT BIAS−2 to OUTPUT V_{CC}−2 across bias resistance
- For channel 4, 5, and 6, connect OUTPUT BIAS to OUTPUT V_{CC}−4,5,6 across bias resistance.

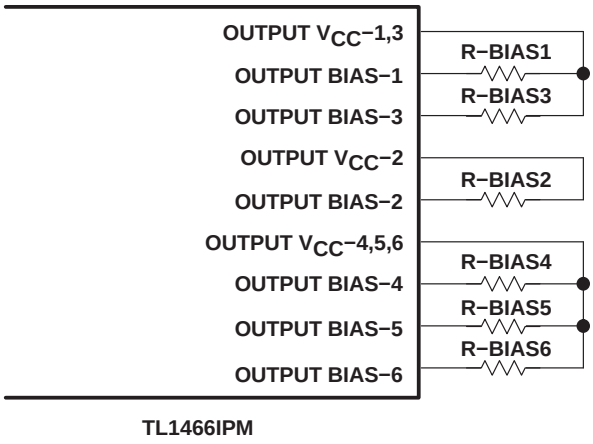
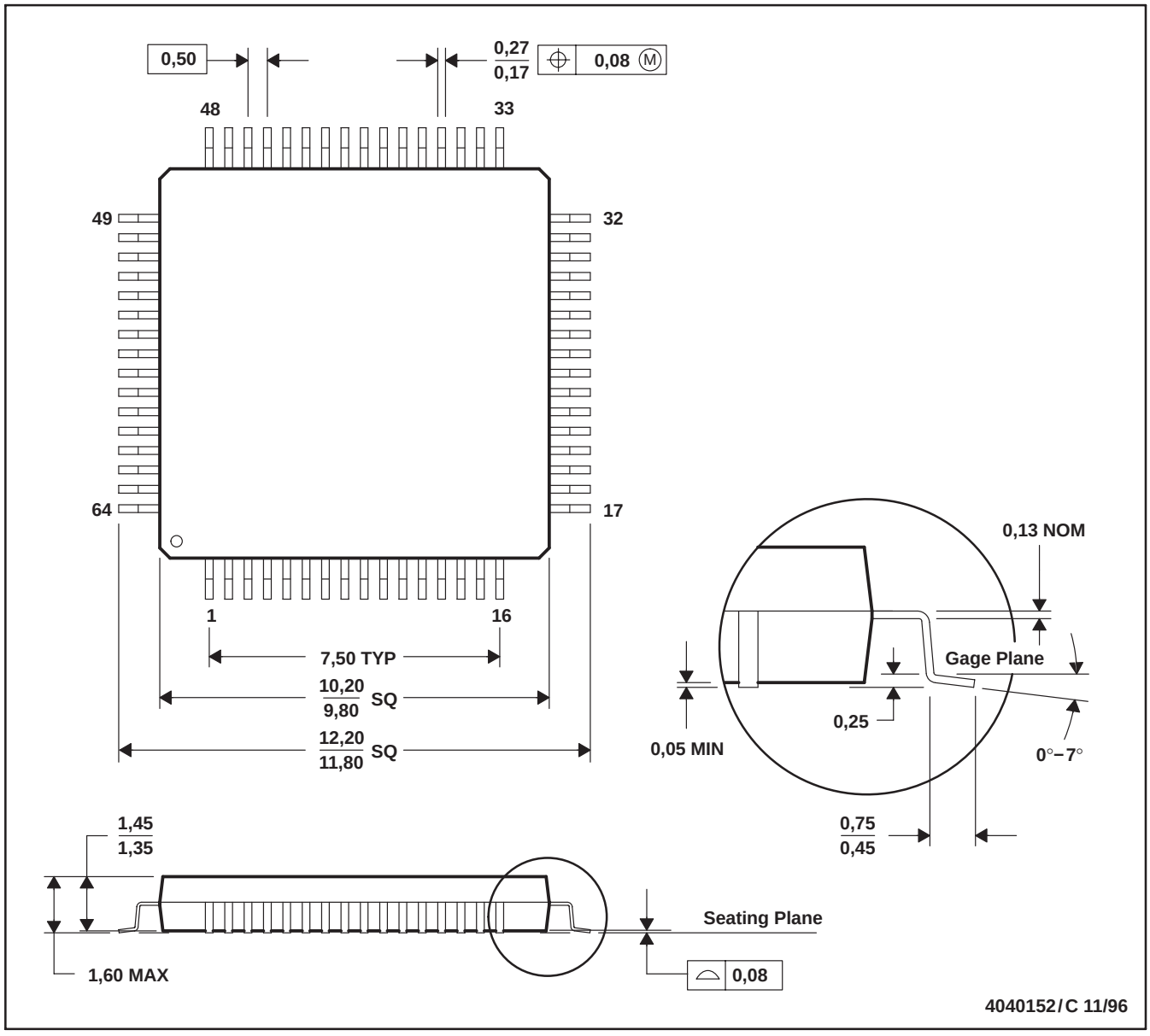


Figure 32. Bias Resistance Connection for Output Sink Current Setting

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL1466IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL1466IPMRG4	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

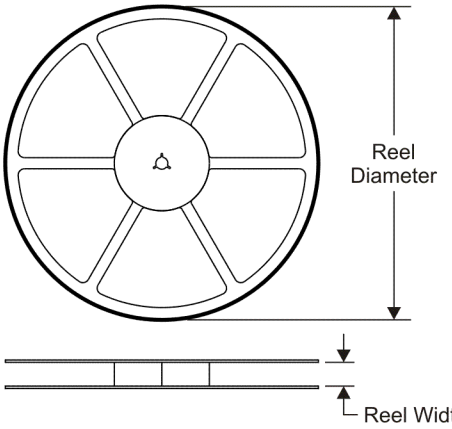
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

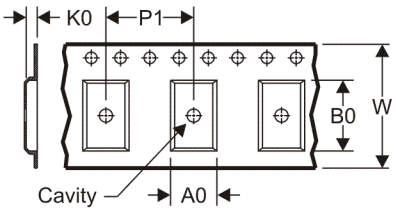
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

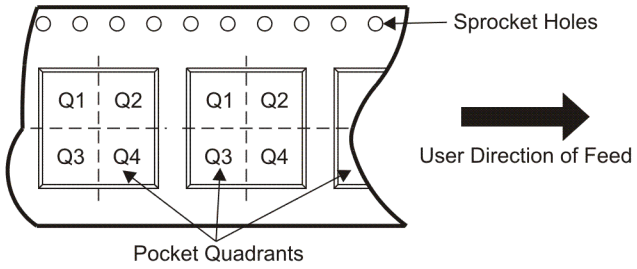


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

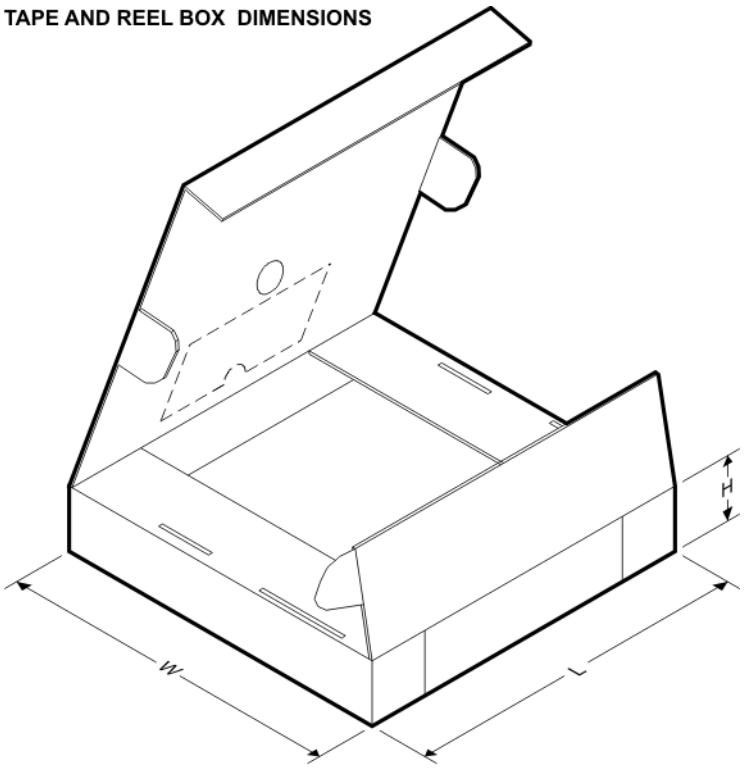
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1466IPMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2

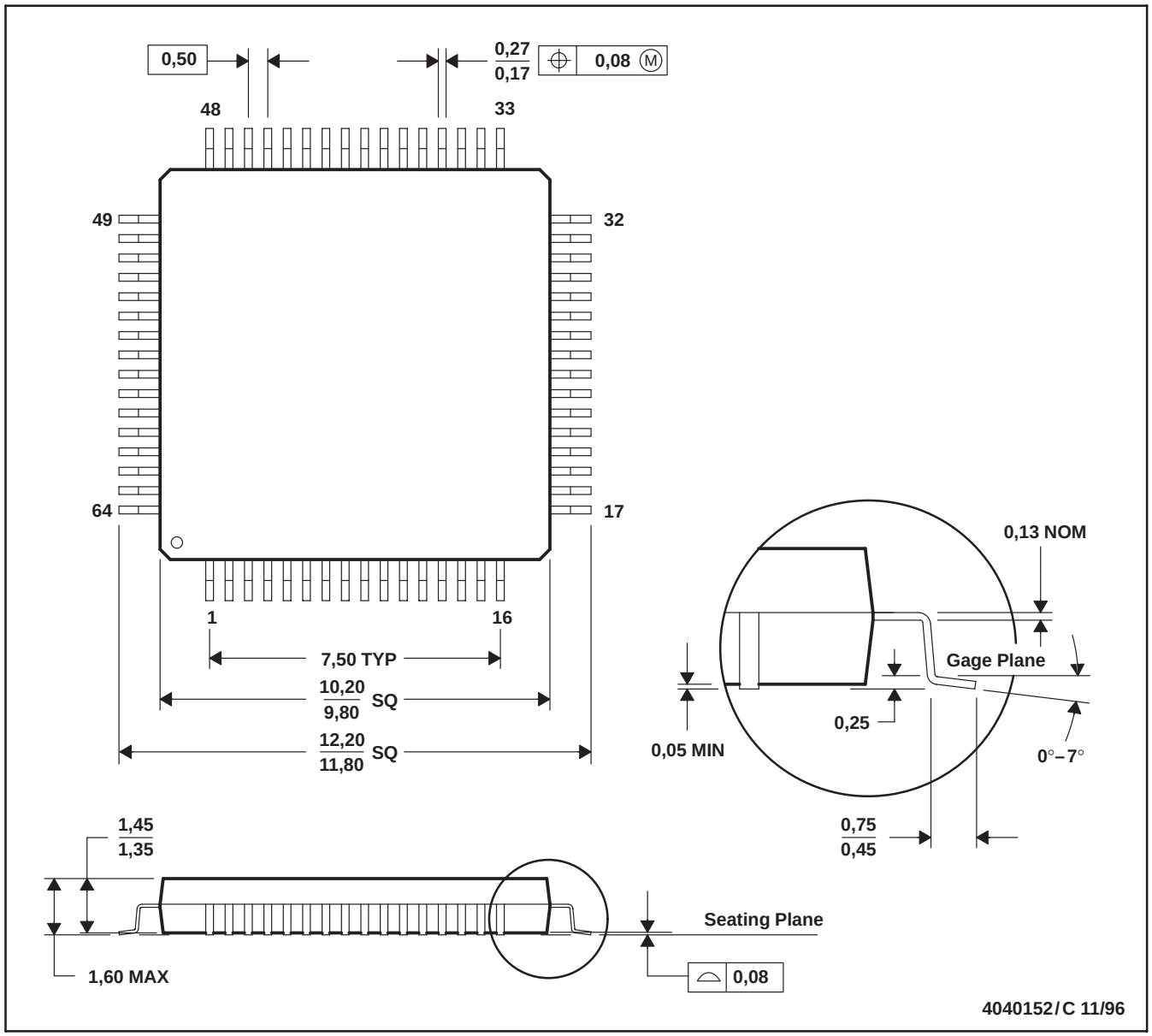
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1466IPMR	LQFP	PM	64	1000	346.0	346.0	41.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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